

## IP Data Sheet

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### 16mA 4V Voltage Regulator

The TS\_VR\_4V00\_X8 is a 4V voltage regulator capable of delivering up to 16mA. It is required for the supply of other TES IPs like TS\_FS\_9M70\_X8, TS\_VA\_LNDC\_X8, and TS\_CS\_20uA\_X8.

The TS\_VR\_4V00\_X8 operates with one supply voltage, VDDA5, VDDIO (5V typical) and one precision reference voltage VREF (2.5V).

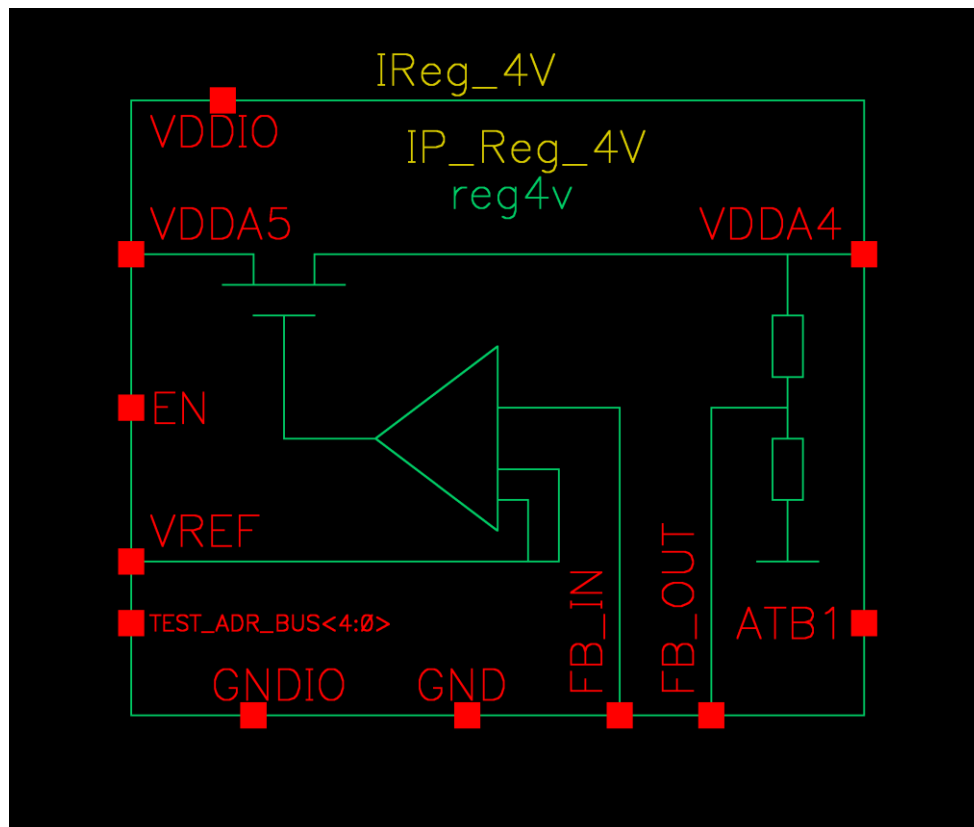
This IP supports analog-test-bus multiplexing on the ATB1 output under control of the 5-bit address input

TEST\_ADR\_BUS<4:0>. When TEST\_ADR\_BUS<4:0>= HHHHL, the TS\_VR\_4V00\_X8 sinks a 1.2µA-internal-bias-replicated current through ATB1 for off-chip measurement.

The TS\_VR\_4V00\_X8 complies with 2kV electrostatic discharges on its analog terminals VDDA4 and ATB1.

The minimum continuous operation lifetime spans 100000 hours.

**Technology:** XFAB XT018 - 0.18µm HV SOI CMOS



## Operating conditions

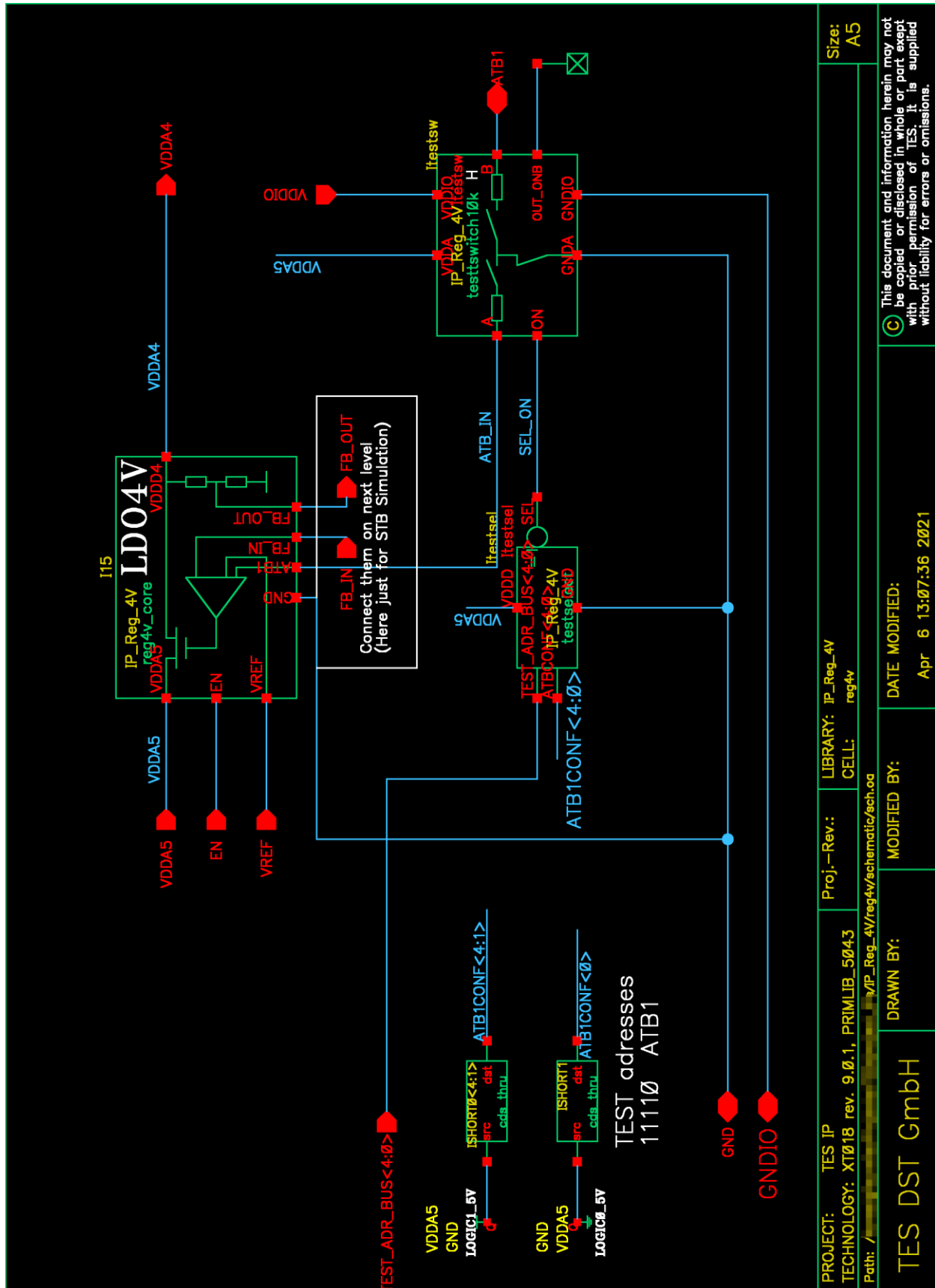
| Parameters                                     | Values                     |
|--|----------------------------|
| Junction temperature range                     | 20°C to +80°C              |
| Supply voltage                                 | VDDA5, VDDIO: 4.9V to 5.1V |
| Reference voltage                              | VREF: 2.5V                 |
| Load current intensity                         | ILOAD: 16mA max            |
| External load capacitor                        | CLOAD: 1.76µF to 2.64µF    |
| EN, TEST_ADR_BUS<4:0> logic-high voltage level | VDDA5                      |

## Specification

| Parameters  | Values               |
|---|----------------------|
| Regulated output voltage                            | 4.00V±0.05V          |
| PSRR over frequencies from DC up to 10 MHz          | 20dB min             |
| Operating power consumption with unloaded output    | 765µW max            |
| Powerdown-mode current consumption<br>Enable EN low | 0.3nA max            |
| Area  | 0.085mm <sup>2</sup> |

FB\_IN and FB\_OUT must be interconnected.

BLOCK DIAGRAM



Size: A5

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|   |                                |                                    |
|---|--------------------------------|------------------------------------|
| PROJECT: TES IP                             | Proj.-Rev.: LIBRARY: IP_Reg_4V | DATE MODIFIED: Apr 6 13:07:36 2021 |
| TECHNOLOGY: XT01B rev. 9.0.1, PRIMLIB_504.3 | CELL: reg4v                    |                                    |
| Path: /IP_Reg_4V/reg4v/schematic/sch.ooc    | MODIFIED BY:                   |                                    |
| <b>TES DST GmbH</b>                         | DRAWN BY:                      |                                    |



LAYOUT VIEW

