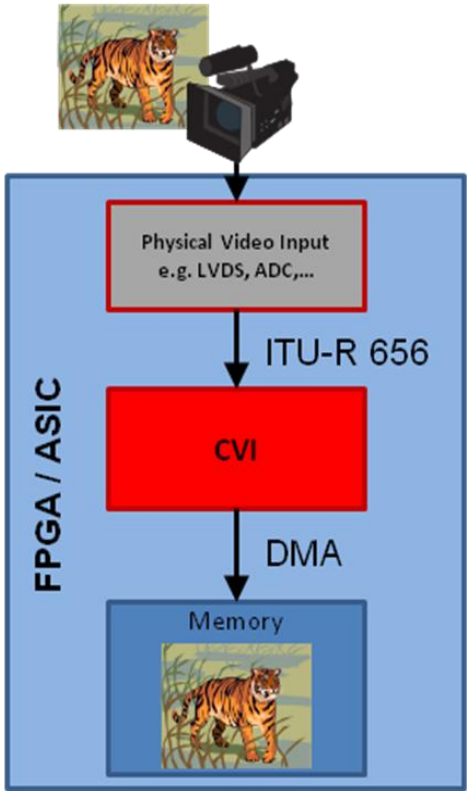
CVI – Configurable Video Input controller IP block

Product Brief

Overview

CVI is a fully **C**ustomizable **V**ideo **I**nput controller IP core. The video input controller can be applied to e.g. FPGA systems with a resource optimized, application specific feature configuration or to ASIC projects applying a more generic feature set and thus more flexibility.



The main functionality of **CVI** is reading an ITU-656 video input stream typically coming from a physical video input interface, e.g. a LVDS PHY or a video ADC, and writing the video data in RGB format to memory via DMA. Several on-the-fly operations on the video data can be applied such as clipping, scaling, color conversion, gamma correction, dithering and de-interlacing.
On the input side CVI can accept RGB as well as YC_BC_R color formats, in the latter case applying the on-the-fly conversion YC_BC_R to RGB.

CVI Customizability

Based on a highly modular architecture the **CVI** offers a wide range of features. The target set of features is configurable at synthesis time, allowing an optimal tailored solution for the target application: not needed features and the related modules are not synthesized, resulting in less resource usage (FPGA logic elements or ASIC gates) and power consumption.

The selected (configured) features can be controlled at run-time via software-programmable registers. To ease the application programmers' life an ANSI-C software driver is delivered providing a set of comfort functions.

CVI Features

Configurable Input Formats

- ITU-R BT.656/BT.601 video-stream (data width 8-10 bits)
- Parallel RGB input

Configurable Output Formats

- RGB656 (16-bit RGB)
- ARGB4444 (16-bit ARGB)
- RGB888 (24-bit RGB)
- ARGB8888 (32-bit ARGB)

Configurable Codeword Correction

- 1-bit error correction,
  2-bit error detection

Frame Detection

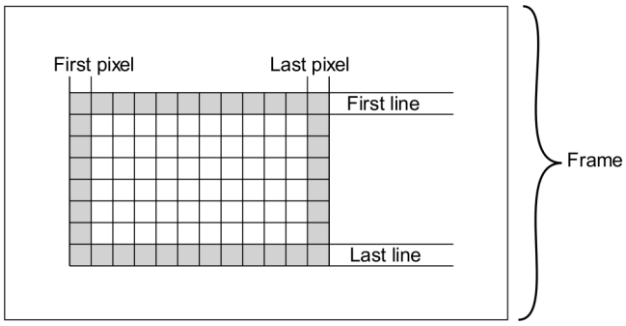
- Detection of valid frame
- Detection of video size (helpful to detect if PAL and NTSC)

Configurable Chroma-Upsampling to YC_BC_R444

- Copying the chrominances of the last pixel (Box-Filter)
- linear interpolation between the chrominances of the last and the next pixel

Configurable Clipping Area

- First pixel of used area
- Last pixel of used area
- First line of used area
- Last line of used area



Configurable Color Adjustment

- Enable or disable the adjustment of saturation, contrast and brightness during the capture

Configurable Colorspace Conversion

- Use a more precise conversion between YC_BC_R and RGB
  - $R = 1.164 * Y' + 1.596 * C_R + 222.921$
  - $G = 1.164 * Y' - 0.392 * C_B - 0.813 * C_R + 135.576$
  - $B = 1.164 * Y' + 2.017 * C_B - 276.836$

Configurable Gamma Correction

- The gamma correction is accomplished via lookup-tables for each RGB channel

Configurable Scaling

- Allows up and downscaling of incoming video
- The scaling also allows two deinterlacing methods (discard and bobbing)

Configurable Deinterlacing

- Weaving (odd and even lines of the video are weaved together)
- Discard (half video-data is scaled to full size of the video)
- Bobbing (Both fields are scaled to the full size of the video)
- None (video is not interlaced or external deinterlacing is done)

Configurable Dithering

- Enable or disable the visual improvement of images with less color Information

Configurable Counter

- Enable or disable line and pixel counter

Power and Control

Configurable Shadowing

- Enable or disable the use of shadow-register to prevent undesired behavior when changing configurations at runtime

Memory blocks controlled by chip select port

Prepared for efficient automatic clock gating

Easy SoC Integration

Low resource consumption

Simple clock domain architecture with four clocks

- Slave bus clock
- Master bus clock
- Processing clock
- Video clock

High bus latency capable (pixel FIFO depth and number of outstanding reads configurable)

Single bus master port (internal arbitration)

Adaptors for common bus protocols

- ARM AMBA: APB for register access,
  AHB or AXI4 for memory bus master access
- Altera Avalon as bus adaptors for both register and bus master access
- Other bus protocols can be easily adapted

Hardware Configuration Support

Comprehensive VHDL configuration package for:

- Configuration of input pixel formats
- Enabling and disabling of certain features at synthesis time
- Configuration of register reset values
- and more

Resource Usage

The footprint (FPGA logic cells or ASIC gate count) strongly depends on the configuration of the **CVI**. The following numbers give an indication of the resource usage for a typical configuration using ITU656 input method with 8-bit channel width, scaling option enabled and a 32-bit bus interface.

Typical FPGA Resource Usage

ALMs	1314
DSP blocks	14
RAM blocks	20

All numbers given for Altera Cyclone V device family

Software Drivers

TES provides a simple basic software driver written in ANSI-C to configure and control the video input controller.

The drivers feature the following characteristics:

- Plain ANSI-C Code
- Fully reentrant & thread-safe
- Minimum OS dependency (HAL part separated), also runs on bare-metal
- No floating point usage
- No inline assembler required
- Small memory footprint

Drivers for other APIs can be developed on request.

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